FAISAL AHMED SHAH

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Education

- **University of Notre Dame**, Notre Dame, Indiana, USA

  PhD in Electrical Engineering. August, 2014.
  GPA: 3.75 out of 4.00.
  Dissertation Title: Integration of Giant Magnetoresistance Stacks with Nanomagnet Logic.

- **Bangladesh University of Engineering & Technology (BUET)**, Dhaka, Bangladesh

  B.Sc. in Electrical and Electronic Engineering. November, 2006.
  GPA: 3.85 out of 4.00.

Honors and Awards

- Professional Development Award, University of Notre Dame Graduate School (2013).
- Departmental Fellowship, University of Notre Dame (2008 - 2009).
- Dean's List Award, Bangladesh University of Engineering and Technology (BUET) (2001-2005).
- University Merit Scholarship, Bangladesh University of Engineering and Technology (BUET) (2001-2004).

Work Experience

- **Graduate Research Assistant**
  University of Notre Dame, Notre Dame, Indiana, USA. (May 2009 - present)

  Current project:

  Current project focuses on realizing a spin valve based electrical output for Nanomagnet Logic (NML).

  - Development of giant magnetoresistance (GMR) stacks and magnetic tunnel junctions (MTJ) using magnetron sputtering systems for nanomagnet logic (NML) applications.
  - Optimization of reactive ion etch and sputter etch processes for dielectrics and magnetic metals.
  - Magnetic annealing of sputtered GMR stacks to introduce exchange bias.
  - Design and development of novel fabrication techniques for nanoscale MTJ and GMR structures.
  - Magnetic and electrical characterization of MTJ and GMR structures.
  - Fabrication of ultra-dense nanomagnets (with sub-10-nm spacing) using double e-beam lithography technique.
  - Micromagnetic simulation of NML elements and NML I/O interfaces.
  - Failure analysis of NML circuits.
  - Modification of a probe station and electronic setup to perform magneto resistance measurement.
  - Development of an UHV magnetic annealing system for introducing exchange bias in GMR structures.
  - Operation and maintenance of a sixteen target UHV sputtering system.

  Other project experiences:

  - Development of a novel substrate independent immobilization method for DNA origami.
  - Design and simulation of CMOS based input driver circuit for nanomagnet logic.
  - Simulation and analysis of high temperature transport property of AlGaN/GaN heterostructure.
  - Design, fabrication and characterization of Diodes, MOSFETS, Inverters, Ring Oscillator and Hall bars.

- **Graduate Teaching Assistant**
  University of Notre Dame, Notre Dame, Indiana, USA. (August 2008 - May 2009)
  - Prepared lecture materials and graded homework and exams for an undergraduate level course.

- **Core Network Operation Engineer**
  Robi Axiata Limited, Dhaka, Bangladesh. (September 2006 - August 2008)
  - Operation and Maintenance of mobile switching centers (MSC).
  - Signal (SS7and IP) and voice traffic (TDM and IP) routing in core network.

Technical Skills

- **Cleanroom Experience:** Over four years' experience of working in class 100 environment.
- **Micro and Nanofabrication Processes and Tools:** Electron Beam Lithography, Photolithography, Mask Making, Metal Evaporation and Sputter, Lift-off, Ion milling, RIE, Wet Etching, Thermal Oxidation, PECVD and other CMOS processes and tools.
- **Measurement, Characterization and Microscopy**: SEM, FIB, AFM, MFM, VSM, CIPT, Parameter Analyzer, XRD, Oscilloscope, Ellipsometer, Surface Profiler.
- **CAD and Simulation Tools**: Cadence CAD Tools, L-Edit, HSPICE, PSPICE, OOMMF.
- **Programming Language**: C/C^{++}, Visual Basic, Matlab, VHDL, Verilog.
- **Operating Systems:** Windows, Linux.

Relevant Graduate Level Courses

- Fundamentals of semiconductor devices
- Fundamentals of semiconductor physics
- Microfabrication beam technology (EBL and SEM)
- Micro & nanomagnetism
- Microelectronic materials
- Transmission Electron Microscopy
- IC fabrication
- Analog circuit design
- VLSI circuit design

Selected Publications & Presentations

- **F. A. Shah**, V. K. Sankar, P. Li, G. Csaba, E. Chen and G. H. Bernstein, "Compensation of Orange-peel Coupling Effect in MTJ Free Layer Via Shape Engineering for NML Applications," ***Journal of Applied Physics*** *115, 17B902 (2014),* DOI: 10.1063/1.4863935.
- **F. A. Shah**, G. Csaba, K. Butler and G. H. Bernstein, "Closely Spaced Nanomagnets by Dual E-beam Exposure for Low-energy NML," ***Journal of Applied Physics*** *113, 17B904 (2013),* DOI: 10.1063/1.4794362.
- **F. A. Shah**, K. N. Kim, M. Lieberman and G. H. Bernstein, "Roughness Optimization of E-Beam Exposed Hydrogen Silsequioxane for Immobilization of DNA Origami," ***Journal of Vacuum Science and Technology B*** *30(1), 011806 (2012),* DOI: 10.1116/1.3676054.
- **F. A. Shah**, K. Butler, G. Csaba, W. Porod and G. H. Bernstein, "IrMn/CoFe/Cu/CoFe-based giant magneto-resistance structure for NML output," ***56th Electronic Materials Conference*** *(EMC), 2014.*
- **F. A. Shah**, V. K. Sankar, P. Li, G. Csaba, E. Chen and G. H. Bernstein, "Compensation of Orange-peel Coupling Effect in MTJ Free Layer Via Shape Engineering for NML Applications," ***58th Annual Conference on MMM****, 2013.*
- **F. A. Shah**, G. Csaba, M. T. Niemier, X. S. Hu, W. Porod and G. H. Bernstein, "Sub-10-nm Inter-magnet Spacing for Improved Defect Tolerance in NML," ***55th Electronic Materials Conference*** *(EMC), 2013.*
- **F. A. Shah**, G. Csaba, K. Butler, G. H. Bernstein, "Closely spaced nanomagnets by dual e-beam exposure for low-energy NML," ***12th Joint MMM / Intermag Conference****, 2013.*
- **F. A. Shah**, V. K. Sankar, G. H. Bernstein, "Fabrication of nanomagnet logic elements using HSQ/Ti/PMMA tri-layer as an etch mask," ***Intermag****, 2012*.